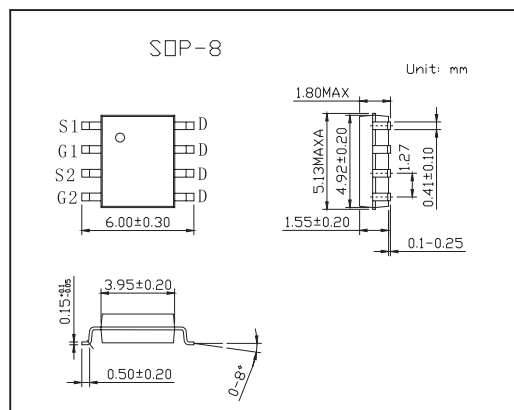
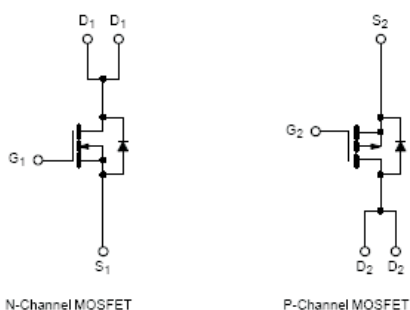


## N-Channel 60-V (D-S), 175°C MOSFET

### KI4559EY

#### ■ PIN Configuration



#### ■ Absolute Maximum Ratings $T_A = 25^\circ\text{C}$

Parameter	Symbol	N-Channel	P-Channel	Unit	
Drain-Source Voltage	$V_{DS}$	60	-60	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$	$\pm 20$	V	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ )* $T_A = 25^\circ\text{C}$	$I_D$	$\pm 4.5$	$\pm 3.1$	A	
		$T_A = 70^\circ\text{C}$	$\pm 3.8$	$\pm 2.6$	A
Pulsed Drain Current	$I_{DM}$	$\pm 30$	$\pm 30$	A	
Continuous Source Current (Diode Conduction)*	$I_S$	2	-2	A	
Maximum Power Dissipation*	$P_D$	$T_A = 25^\circ\text{C}$		2.4	W
		$T_A = 70^\circ\text{C}$		1.7	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 175		$^\circ\text{C}$	
Maximum Junction-to-Ambient *	$R_{thJA}$	62.5		$^\circ\text{C}/\text{W}$	

\*Surface Mounted on FR4 Board,  $t \leq 10$  sec.

## KI4559EY

■ Electrical Characteristics T<sub>J</sub> = 25°C

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit	
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	N-Ch	1		V	
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	P-Ch	-1			
Gate Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V	N-Ch		±100	nA	
		V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V	P-Ch		±100		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0 V	N-Ch		2	μA	
		V <sub>DS</sub> = -60V, V <sub>GS</sub> = 0 V	P-Ch		-2		
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55°C	N-Ch		25	μA	
		V <sub>DS</sub> = -60V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55°C	P-Ch		-25		
On State Drain Currenta	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	N-Ch	20		A	
		V <sub>DS</sub> ≤ -5 V, V <sub>GS</sub> = -10 V	P-Ch	-20			
Drain Source On State Resistance*	r <sub>Ds(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4.5A	N-Ch		0.045	0.055	Ω
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -3.1A	P-Ch		0.100	0.120	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 3.9A	N-Ch		0.055	0.075	
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -2.8A	P-Ch		0.125	0.150	
Forward Transconductance*	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 4.5A	N-Ch		13	S	
		V <sub>DS</sub> = -15 V, I <sub>D</sub> = -3.1A	P-Ch		7.5		
Diode Forward Voltage*	V <sub>SD</sub>	I <sub>S</sub> = 2A, V <sub>GS</sub> = 0 V	N-Ch		0.9	1.2	V
		I <sub>S</sub> = -2A, V <sub>GS</sub> = 0 V	P-Ch		-0.8	-1.2	
Total Gate Charge	Q <sub>g</sub>	N-Channel V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 4.5A	N-Ch		19	30	nC
Gate Source Charge	Q <sub>gs</sub>	P-Channel V <sub>DS</sub> = -30 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -3.1A	N-Ch		4		
Gate Drain Charge	Q <sub>gd</sub>		N-Ch		3		
		P-Ch		1.6			
Turn On Time	t <sub>d(on)</sub>	N Channel V <sub>DD</sub> = 30 V, R <sub>L</sub> = 30 Ω	N-Ch		13	20	ns
Rise Time	t <sub>r</sub>	I <sub>D</sub> = 1A, V <sub>GEN</sub> = 10V, R <sub>g</sub> = 6 Ω	P-Ch		8	15	
			N-Ch		11	20	
Turn Off Delay Time	t <sub>d(off)</sub>	P-Channel V <sub>DD</sub> = -30 V, R <sub>L</sub> = 30 Ω	N-Ch		36	60	
			P-Ch		12	25	
Fall Time	t <sub>f</sub>	I <sub>D</sub> = -1 A, V <sub>GEN</sub> = -10 V, R <sub>g</sub> = 6 Ω	N-Ch		11	20	
			P-Ch		35	50	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 2 A, di/dt = 100 A/μs	N-Ch		35	60	
		I <sub>F</sub> = -2 A, di/dt = 100 A/μs	P-Ch		60	90	

\* Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.